 

**Machine Learning for Better Thermal Management:** Thermal management is one of the most critical issues impacting the performance and reliability of next-generation electronics packaging technologies. That’s because new architectural features such as backside power delivery networks (BSPDNs) and 3D IC configurations introduce new components within the thermal pathway, creating additional heat dissipation challenges. To optimize thermal management, better estimation of chip and package temperatures is required. But while analytical approaches to estimate BEOL interconnect-layer thermal resistance have been developed, they are inadequate. At ECTC, IBM researchers will describe how they used a series of finite element modeling (FEM) simulations to train a machine learning (ML) model to rapidly predict the thermal resistance of BEOL stacks in a test chip. BEOL layout design, heights and material information were used as inputs. The researchers say the ML model predicted the thermal resistance of BEOL stacks with a mean absolute percentage error (MAPE) of less than 15%. That is a remarkable accuracy improvement versus the traditional 1-D heat conduction analytical model used for comparison, which showed a MAPE of 300%. The machine learning approach opens the possibility of more accurate predictions of hotspots in advanced packaging architectures, thus helping to increase their performance and reliability.

* **At left above** are a series of schematics showing increasingly complex thermal pathways in (a) a 2D front-side power delivery network (FSPDN) package; (b) a 2D BSPDN; and (c) a 3D IC package with two dies.
* **At right above** is a representative 3D BEOL sub-stack model with (a) dielectrics included and (b) dielectrics removed for visualization. (c) is a schematic of the finite element model setup for thermal resistance extraction, and (d) is a representative temperature profile in the metal.

**(IP session #37, “*Fast And Accurate Machine Learning Prediction of Back-End-Of-Line Thermal Resistances in Backside Power Delivery and Chiplet Architectures*,” P. Chowdhury et al, IBM)**